WHAT IS CLAIMED IS:

1. A thin film transistor, comprising:

a substrate having an upper side;

a plurality of active layers over the upper side;

spaces defined between the substrate and the active layers;

a first insulating layer on the plurality of active layers;

a gate electrode on the first insulating layer over the plurality of active layers; and

source and drain electrodes contacting the plurality of the active layers.

2. The thin film transistor of claim 1, wherein the spaces are formed by etching the upper side of the substrate.

3. The thin film transistor of claim 1, wherein the ends of the active layers contact the upper side of the substrate.

4. The thin film transistor of claim 1, further comprising a second insulating layer over the gate electrode and the active layers, the second insulating layer having contact holes penetrating to the active layers, wherein the source and drain electrodes contact the active layers through the contact holes.

5. The thin film transistor of claim 1, wherein the source and drain electrodes are under the active layers.

6. The thin film transistor of claim 1, wherein multiple spaces are under an active layer.

7. The thin film transistor of claim 1, further including a pier between an active layer and the substrate, wherein the pier supports an active layer.

8. The thin film transistor of claim 7, wherein the pier is between spaces.

9. The thin film transistor of claim 1, further comprising a space-forming layer having the space between the active layers and the substrate.

10. The thin film transistor of claim 9, wherein the ends of the active layers contact the space-forming layer.

11. The thin film transistor of claim 5, further comprising doped source and drain regions on the source and drain electrodes, respectively, wherein the doped source and drain regions are amorphous silicon and contact the active layers.

12. The thin film transistor of claim 1, wherein said plurality of active layers are connected in parallel.

13. The thin film transistor of claim 12, wherein each of said plurality of active layers includes a drain region, a source region, and a channel region.

14. The thin film transistor of claim 12, wherein each of said plurality of active layers is polysilicon.

15. The thin film transistor of claim 14, wherein the polysilicon is comprised of a central region having relatively large crystal grain sizes and end regions comprised of relatively small crystal grain sizes.

16. A method of fabricating a thin film transistor, comprising:

providing a substrate;

depositing amorphous silicon on the substrate;

patterning the amorphous silicon to form plural island-shaped amorphous silicon layers;

forming spaces between the substrate and the amorphous silicon layers;

forming a channel region, a source region, and drain ohmic contact regions on each of the amorphous silicon layers by ion doping the island-shaped amorphous silicon layers;

forming a first insulating layer over the amorphous silicon layers;

crystallizing the amorphous silicon layers to form polysilicon layers by irradiating laser beams onto the first insulating layer;

forming a gate electrode on the first insulating layer; and

forming source and drain electrodes that contact the source and drain ohmic contact regions, respectively.

17. The method of claim 16, wherein the forming of the channel region, the source region, and the drain ohmic contact regions on each of the amorphous silicon layers is performed by forming ion stoppers on the island-shaped amorphous silicon layers, using the ion stoppers as masks during doping, and then removing the ion stoppers.

18. The method of claim 16, wherein the spaces are formed by etching an upper side of the substrate.

19. The method of claim 16, wherein the spaces are formed by depositing a space-forming layer between the substrate and the amorphous silicon, and then patterning the space-forming layer to form the spaces therein.

20. The method of claim 16, wherein the source and drain electrodes are formed under the active layers.

21. The method of claim 16, further including forming a second insulating layer on the gate electrode such that the second insulating layer includes contact holes that expose the source and drain ohmic contact regions.

22. The method of claim 21, further including forming source and drain electrodes on the second insulating layers that contact the active layers via the contact holes.

23. The method of claim 20, further including forming doped source and drain regions having island-shapes on the source and drain electrodes.

24. The method of claim 23, wherein the source and drain regions are formed of amorphous silicon.

25. The method of claim 23, wherein the source and drain regions are formed in contact with the plurality of active layers.

26. A display array, comprising:

a substrate having an upper side;

a CMOS transistor having an N-type TFT and a P-type TFT that are formed over said upper side; and

a thin film switching transistor over said upper side and that is in electrical communication with said CMOS transistor, said thin film switching transistor including;

a plurality of polysilicon active layers over the upper side;

spaces defined between the substrate and the active layers;

a first insulating layer on the plurality of active layers;

a gate electrode on the first insulating layer over the plurality of active layers; and

source and drain electrodes contacting the plurality of the active layers.

27. A display array according to claim 26, wherein said N-type TFT has a polysilicon

active layer.

28. A display array according to claim 27, further including a space defined between the substrate and the polysilicon active layer of N-type TFT.

29. A display array according to claim 27, further including a pixel element over said substrate.